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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,978	10/18/2004	Paul H. Bergeron	BUR920040134US1	5977

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EXAMINER	
WHITMORE, STACY	
ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/711,978	BERGERON ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5,6,8 and 11-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,11-13,16,18-20,23,25-28 and 31-33* is/are rejected.

7)☒ Claim(s) *6,8,14,15,17,21,22,24,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: Claim 1 comprises the claim language "wherein the method one of" that is grammatically incorrect. Applicant appears to mean "wherein the method comprises one of". Appropriate correction is required.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1,5,11-13,16,18-20,23,25-28 and 31-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Su, J.Z.; et al., "Post-route optimization for improved yield using a rubber-band wiring model". Su was cited by applicant on the IDS dated November 12, 2004.

4. As for the claims, Su discloses the invention as claimed, including:

[Claim 1] 1. A method of modifying circuit design source data of a three- dimensional structure for improving integrated circuit yield, the method being implemented with computer program code and hardware [pg. 706, section 5. shows the design process run on a Sun Sparc 20] and comprising the steps of:
locating a problem structure remaining after post-layout optimizing using a shapes-processing tool [abstract, pg. 702, section 2; pg. 704, section 3. – the problem structure are the spot defects];
implementing at least one local modification to said three- dimensional structure to perform a fix-up process on the problem structure [abstract, pg. 702, section 2; pg. 704, section 3. – the local modification is the spreading of the wires located over the spot defects];

wherein the method one of:
introduces jogs in wires of one layer arranged above wires of another layer [pg. 701, figs. 1-2, and left hand side – the flexibility of the wire is provided by the rubber-band updating, and the jog is the movement of the wire by the rubber-band process; pg. 701 left hand side also shows that the RBU handled multiple layers and different signal (wiring layers). The claim language does not require the introduction of the jogs of the one layer above wires of another layer be related in any way. The introduction of the jog, therefore could be for any reason. The only claim language requirement is that the jog in wires are arranged over another wiring layer];
introduces segments of wrong-way wiring in wires of one layer arranged above wires of another layer [];
increases a space of minimum-spaced wires over a wider structure [pg. 702, section 2, spot defects, wherein the spot defect is any extra or missing material, which would be under the wiring layer under consideration, may comprise material such as missing or extra wiring material, and the missing material may be considered a trench; the incompatible structure is the spot defect, and the spot defect is determined by its larger (wider size) in relation to the spacing of wires (which are above it); pg. 704, section 3];
forms a dummy hole in an incompatible structure component of a first layer of the problem structure to reduce manufacturing defects of a structure component in a second layer of the problem structure []; and
widens a trench of a lower layer of the problem structure under at least one wire of an upper layer of the problem structure [];
[Claim 5] 5. The method of claim 1, wherein the wider structure comprises an incompatible structure component of the problem structure [abstract, pg. 702, section 2 – the incompatible structure is the spot defect, and the spot defect is determined by its larger (wider size) in relation to the spacing of wires (which are above it); pg. 704, section 3];
[Claim 11] 11. A method of modifying circuit design source data for forming a multi-layer structure of a semiconductor device, comprising the steps of:

determining whether at least two minimum-spaced wires of an upper layer pass over a dishing-prone structure of a lower layer [abstract, pg. 702, section 2; pg. 704, section 3. – the local modification is the spreading of the wires located over the spot defects, the dishing prone structure is the structure that would leave the spots of missing material on the wafer]; and
if so performing at least one of:
increasing a space between the two minimum-spaced wires of the upper layer in a region over the dishing-prone structure of the lower layer [section 2; pg. 704, section 3.];
forming a dummy hole in a wide wire under the space between the two minimum-spaced wires; and widening a trench between two wide wires under the space between the two minimum-spaced wires [];
wherein the method is implemented with computer program code and hardware [pg. 706, section 5. shows the design process run on a Sun Sparc 20];

Note that the "if so" limitation of claim 11 inherently includes the "if not" situation, and therefore, the increasing and forming steps are not required by the claim language.

[Claim 12] 12. The method of claim 11, further comprising increasing the flexibility of at least one wire of the two minimum-spaced wires above the dishing-prone structure [abstract, pg. 706, section 5, minimum wire to wire design rule, pg. 701 flexibility of the RBU; pg. 702, section 2 – the incompatible structure is the spot defect, and the spot defect is determined by its larger (wider size) in relation to the spacing of wires (which are above it); pg. 704, section 3];
[Claim 13] 13. The method of claim 12, wherein increasing the flexibility of the at least one wire of the two minimum-spaced wires comprises forming at least one jog in the at least one wire [abstract, pg. 706, section 5, minimum wire to wire design rule, pg. 701 flexibility of the RBU; pg. 702, section 2 – the incompatible structure is the spot defect, and the spot defect is determined by its larger (wider size) in relation to the spacing of wires (which are above it); pg. 704, section 3pg. 701, figures 1 and 2 shows jogs of the RBU];

[Claim 16] 16. The method of claim 11, further comprising causing a router to reroute at least one wire of the at least two minimum-spaced wires [abstract, pg. 702, section 2; pg. 704, section 3. – the local modification is the spreading of the wires located over the spot defects, further pg. 702, first full paragraph shows the SURF tool as a router which uses the rubber-band wiring or re-routing; and also pg. 706, section 5., minimum wire to wire design rules which apply to the design system of Su];

[Claim 18] 18. A method of modifying circuit design source data of a three-dimensional structure for forming a multi-layer structure of a semiconductor device, comprising the steps of:

forming a dishing-prone structure on a lower layer [pg. 702, section 2, the dishing prone structure is the structure causing the missing material on the wafer];

forming two minimum-spaced wires over the dishing-prone structure on an upper layer [pg. 704, section 3]; increasing a space between the two minimum-spaced wires in a region over the dishing-prone structure [pg. 704, section 3];

wherein the method is implemented with computer program code and hardware [pg. 706, section 5. shows the design process run on a Sun Sparc 20];

Note that the "if" claim language inherently includes the "if not" situation, and therefore the claim language as part of the "if" situation is not required to be rejected.

if the dishing-prone structure includes a wide wire, inserting a space for a dielectric island in the wide wire under at least one wire of the two minimum- spaced wires; and

if the dishing-prone structure includes a narrow trench between two wide wires, widening the narrow trench under of the space between the two minimum-spaced wires [];

[Claim 19] 19. The method of claim 18, further comprising increasing the flexibility of at least one wire of the two minimum-spaced wires proximate the dishing-prone structure [see as cited in the rejection of claim 12];

[Claim 20] 20. The method of claim 19, wherein increasing the flexibility of the at least one wire comprises forming at least one jog in the at least one wire of the two minimum-spaced wires [see as cited in the rejection of claim 13];

[Claim 23] 23. The method of claim 18, further comprising causing a router to reroute at least one wire of the at least two minimum-spaced wires [see as cited in the rejection of claim 16];

[Claim 25] 25. Circuit design source data for a multi-layer structure of a semiconductor device, comprising:

an upper layer comprising multiple minimum-spaced wires [pg. 702, section 2.; pg. 704, section 3];

a lower layer comprising a dishing-prone structure, wherein the multiple minimum-spaced wires of the upper layer are disposed over the dishing-prone structure of the lower layer [pg. 702, section 2.; pg. 704, section 3]; an increased space between at least two wires of the multiple minimum- spaced wires in a region over the dishing-prone structure [pg. 702, section 2.; pg. 704, section 3];

wherein the method is implemented with computer program code and hardware [pg. 706, section 5. shows the design process run on a Sun Sparc 20];

Note that the "if" claim language inherently includes the "if not" situation, and therefore the claim language as part of the "if" situation is not required to be rejected.

a dummy hole in the wide wire under at least one wire of the multiple minimum-spaced wires if the dishing-prone structure includes a wide wire; and a widened region of the narrow trench under at least one wire of the multiple minimum-spaced wires if the dishing-prone structure includes a narrow trench between two wide wires [];

[Claim 26] 26. The circuit design data of claim 25, comprising a jog in at least one wire of the multiple minimum-spaced wires proximate the dishing- prone structure [see as cited in the rejection of claim 12];

[Claim 27] 27. The circuit design data of claim 26, comprising at least two jogs in at least one wire of the multiple minimum-spaced wires proximate the dishing-prone structure [see as cited in the rejection of claim 12];
[Claim 28] 28. The circuit design data of claim 25, wherein an increased space between at least two wires of the multiple minimum-spaced wires comprises an adjustable shape between the at least two wires of the multiple minimum-spaced wires [pg. 701, figs. 1-2, the adjustable shape as claimed may just be the shape that is between the wires and not necessarily another entity between the wires; also pg. 700, section 1. – adjust locations of movable objects, which reads as an adjustable shape];
[Claims 31-32] wherein the wider structure comprises a wider wire or trench [pg. 702, section 2, spot defects, wherein the spot defect is any extra or missing material, which would be under the wiring layer under consideration, may comprise material such as missing or extra wiring material, and the missing material may be considered a trench; the incompatible structure is the spot defect, and the spot defect is determined by its larger (wider size) in relation to the spacing of wires (which are above it); pg. 704, section 3];
[Claim 33] wherein the locating a problem structure using shapes processing tool comprises locating a problem structure remaining after post-layout optimizing using the shapes processing tool [pg. 702, section 2. – the location of the defects is the location of a problem structure which must use some sort of shape processing tool in order to detect defects in materials].

5. Claims 6, 8, 14-15, 17, 21-22, 24, and 29-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to disclose either singularly or in combination the invention as claimed, including a method for modifying circuit design source data comprising at least wherein increasing a space of two minimum spaced wires comprises

forming a dummy shape between the at least two wires and increasing the size of the dumpy shape; wherein forming a dummy hole comprises forming a gap in the incompatible structure; wherein increasing a space between the two minimum-spaced wires comprises forming a dummy shape between the two wide wires by increasing the width of the dummy shape; wherein forming the dummy hole in the wide wire comprises forming a gap configured to be filled with a dielectric in the wide wire approximately perpendicular to a long axis of the at least one wire of the two minimum-spaced wires; wherein widening the trench under the space between the two minimum-spaced wires comprises narrowing at least one wide wire of the two wide wires; wherein increasing a space between the two minimum-spaced wires comprises forming a dummy shape between the two minimum-spaced wires and increasing the width of the dummy shape; wherein forming a dielectric island configured to be filled with a dielectric in the wide wire comprises forming a gap in the wide wire approximately perpendicular to a long axis of the at least one wire of the two minimum-spaced wires; wherein widening the narrow trench under at least one wire of the two minimum-spaced wires comprises narrowing at least one wide wire of the two wide wires; wherein the adjustable shape in the wide wire comprises a gap in the wide wire approximately perpendicular to a long axis of the at least one wire of the multiple minimum-spaced wires; and wherein a widened region of the narrow trench comprises a narrow region of at least one wide wire of the two wide wires.

7. Applicant's arguments filed 4/24/2007 have been fully considered but they are not persuasive.

In the remarks applicant argues in substance:

A: Su does not disclose the claimed limitations of claims 1, 11, 18, and 25.

8. Examiner disagrees for the following reasons:

As to A: Su discloses the elements of claims 1, 11, 18, and 25, and dependent claims [please see the cited portions of claims as examiner has included explanations of the cited portions of the reference and how the reference relates to the claim language].

9. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stacy A Whitmore/
Primary Examiner
Art Unit 2825

SAW
July 8, 2007